# PLC-clock user manual

(english)
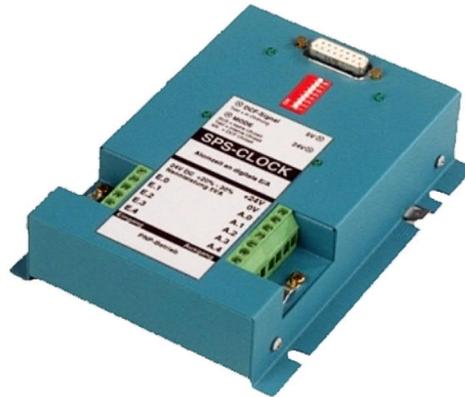


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# index of contents

## PLC-clock

# 7 Technical data

# PLC-clock

# 1 Description

The SPS-Clock is a DCF receiver. With the digital I / O of the PLC, the atomic time can be received. All you need is some of the inputs and outputs of your PLC and a program in your PLC, to query the PLC clock and deposite the time in a DB. The program is described in this manual.

The following time information are available:

- second
- minute
- hour
- day
- month
- year (2-digit)
- weekday (Mo,Di,...)
- Status bits (DCF OK, summer time, winter time, ..)

# 2 System requirements

## 2.1 Software

- Program in the PLC to query the PLC Clock (described in the "Configuration" )

## 2.2 Hardware

- 5 digital inputs to the PLC
- 5 digital outputs to the PLC
- DCF antenna
- optional amplifier
- 24V DC power supply

# 3 Connecting options

Atomic time / clock at the PLC
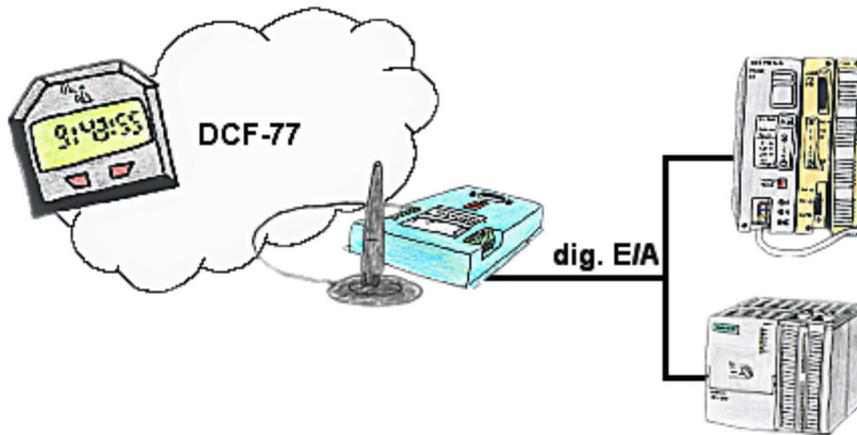
# 4 Installation

## 4.1 Hardware

Connection to PLC:
connect PLC inputs of the CLOCK with the digital outputs of the PLC
connect PLC outputs of the CLOCK with the digital inputs of the PLC
PLC clock with +24 V voltage supply.

The functions are accessed as needed by the PLC and are normally (except for extremely fast polling of the PLC) not time critical. In- and outputs should be connected to the PLC bit compatible. When using the sample PLC software it is strictly necessary.

Inputs: Control via +24 V (logical 1)
No signal corresponding to 0V (log.0)

Outputs: In log.1 be switched +24 V
In log.0 is no switching through

Note: In the current version (1.0) of the PLC CLOCK can be done without the input bit 4 as the corresponding registers are not used.

# 5 Control elements

## 5.1 Status LEDs

**DCF-Signal**     **5V**
Takt = in Ordnung

**MODE**     **24V**
AUS = keine Uhrzeit
Takt = interne Uhrzeit
AN  = DCF Uhrzeit
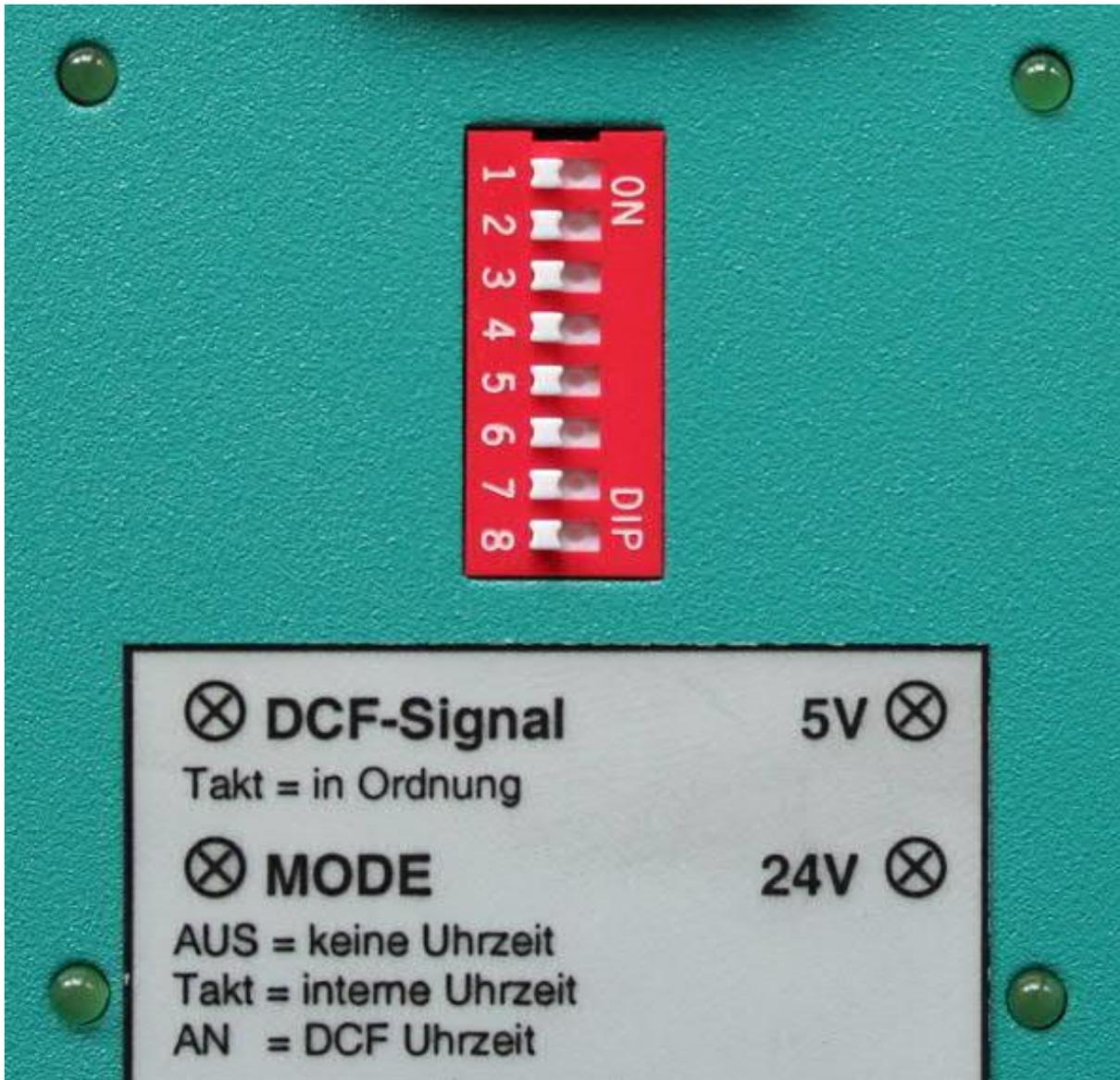
**DCF signal LED:**

Green LED off:
no DCF signal is received

Green LED blinking:
DCF signal is received

**5V LED:**

Green LED off:
Internal 5V are not generated

Green LED on
Internal 5V are generated and available

**Fashion LED:**

Green LED off:
no valid time available i.e. the clock has not synchronized itself after switching to a DCF signal

**24V LED:**

Green LED off:
24V power supply is not connected to the device

Green LED blinking:
freewheeling (quartz) clock in operation
i.e. the DCF signal is not available
currently valid. Internal clock was
synchronized 1x and continues. Status
bits will not be issued. Summer / winter
time changes are not made.

Green LED on:
In DCF mode, all data are taken from
the sender (atomic time). Status bits are
outputted. Summer / winter time
changes are made automatically.

Green LED on:
24V power supply is connected to the
device

## 5.2 DIP switch

The DIP switches are reserved for future use and must be set to "0" (off)d uring normal
operation. If one or several DIP switches set to "1" (ON), it can cause a malfunction.

# 6 Configuration

## 6.1 Reading out the register

The registers (see table) will be read out as follows:

1. (E) "0" Output
2. (E) '00000' Test
3. (N) register outputting
4. (N) wait approx. 50 ms (depends on the periphery of the PLC, PLC CLOCK reacts after 2ms)
5. (N) value queries
6. (N) parity evaluation
7. more queries

(N) = necessary steps for the query
(E) = recommended steps for safe query

### 6.1.1 Register data

Time information can be read via the following registers:

| register number | function | valence |
|---|---|---|
| 0 | no function, feedback | 0 0 0 0 0 |
| 1 | status bits | P W W W W |
| 2 | seconds (Bit 0-3) | P W W W W |
| 3 | Sekunden (Bit 4-7) | P W W W W |
| 4 | minutes (Bit 0-3) | P W W W W |
| 5 | minutes (Bit 4-7) | P W W W W |

| 6 | hours (Bit 0-3) | P W W W W |
|---|---|---|
| 7 | hours (Bit 4-7) | P W W W W |
| 8 | days (Bit 0-3) | P W W W W |
| 9 | days (Bit 4-7) | P W W W W |
| 10 | days (Bit 0-3) | P W W W W |
| 11 | days (Bit 4-7) | P W W W W |
| 12 | years (Bit 0-3) | P W W W W |
| 13 | years (Bit 4-7) | P W W W W |
| 14 | weekday | P W W W W |
| 15 | not assigned | 0 1 1 1 1 |
| 16 | not assigned | |
| 17 | not assigned | |
| 18 | not assigned | |
| 19 | not assigned | |
| 20 | not assigned | |
| 21 | not assigned | |
| 22 | not assigned | |
| 23 | not assigned | |
| 24 | not assigned | |
| 25 | not assigned | |
| 26 | not assigned | |
| 27 | not assigned | |
| 28 | not assigned | |
| 29 | not assigned | |
| 30 | not assigned | |
| 31 | not assigned | |

P = Parity bit (odd)
W = data value

The registers 2-13 are divided in binary values (bit 7 and 3 .4 .0)

### 6.1.1.1 Status bits

Secondary antenna is on the transmitter in Mainfingen / Offenbach
1 = DCF operation of the PLC-CLOCK
2 = UTC + 2h (EET / Summer Time)
3 = UTC + 1h (CET / winter time)

### 6.1.1.2 Weekday

1 = monday
2 = tuesday
3 = wednesday
4 = thursday
5 = friday
6 = saturday
7 = sunday

## 6.2 PLC program

The test program included on the CD in \ LICENSE \ PLC CLOCK \ is freely programmable and changeable. It cyclically transmits all data in the working DB (DW9-16). If you do not require all the data so you can adjust the block (FB99) easily to your needs.

### 6.2.1 Data (labor) DB

The number of the DB must be specified before calling the FB99 (see FB1)

DB 099 File: SPSCLKST.S5D LAE = 25

Data block for PLC CLOCK
0: KH = 0000;
1: KF = +00000; Internal step sequence
2: KF = +00000; Request delivery of internal registers
3: KH = 0000;
4: KH = 0000;
5: KH = 0000;
6: KH = 0000;
7: KH = 0000;
8: KH = 0000;
9: KM = 00000000 00000000; status bits
10: KF = +00000; seconds
11: KF = +00000; minutes
12: KF = +00000; hours
13: KF = +00000; days
14: KF = +00000; months
15: KF = +00000; years
16: KF = +00000; weekday
17: KH = 0000;
18: KH = 0000;
19: KH = 0000;

### 6.2.2 OB1

OB1 is here only to start the program, it requires example FB1

OB File 001: SPSCLKST.S5D LAE = 9

Network 1 of 1
:SPA FB 1
name :MAIN
:
:BE

### 6.2.3 Example: FB for FB99 (FB1)

The FB1 has the following functions:

- Takeover of inputs (MB200)

- Award of the DB number (before FB call)
- Parameterization of the FB (TD + TO)
- Takeover of outputs (MB201)

The number of FB's is arbitrary.
The FB99 call can be done by SPA or SPB.
A multi-call is possible in the program.

FB 001 file: SPSCLKST.S5D LAE=28

network 1 of 1

name : MAIN

```
        : L             EB 0        - inputs of PLC CLOCK
        : T             MB 200   in SME
        : L             KF 99       - work-DB
        : SPA           FB 99
name : SPSCLOCK
TD    : T 98
TO    : T 99
        : L             AB 1        - is not used Bit 4
        : L             KH 00E0 here can stand also 00F0
        : UW
        : L             MB 201   - outputs from SME handed over
        : OW
        : T             AB 1
        : BE
```

## 6.2.4 PLC CLOCK function block (FB99)

The FB99 has the following functions:

- Sampling of each tab
- Parity checking on the values
- Put together and takeover the values ??in the data words

The number of FB's is arbitrary.
In Network 5 can the block to be transferred easily influenced (upper lower limit)

FB 099 file: SPSCLKST.S5D LAE=141

network 1 of 6

name : SPSCLOCK

```
Bez   : TD             E/A/D/B/T/Z: T
Bez   : TO             E/A/D/B/T/Z: T
        : T             MW 240         - safe work-DB
        : B             MW 240         and open
        : A             DB 0
        : L             MB 200         - not for SPS-Clock / hide unused bits
        : L             KH 001F
        : UW
        : T             MB 200
        : U             M 212.0        - VKE produce 0 Bit
        : R             M 212.0
        : ***
```

network 2 of 6 "zero" and "error" signal evaluation
```
        : L             KH 0000
        : L             MB 200
        : !=F
        : =             M 212.1        "zero"-signal
        : L             KH 000F
        : !=F
        : =             M 212.2
        : ***
```
network 3 of 6 step 0 / issue "0"
```
        : L             DW 1
        : L             KF 0
        : ><F
        : SPB           =M001
        : L             KH 0000        - output "0"
        : T             MB 201
        : L             KH 0000        - if "zero" for an answer then next step
        : ><F
        : SPB           =M001
        : U             M 212.0
        : SE            =TD            - timer reset
        : L             KF 1
        : T             DW 1           - next step
M001    : ***
```
network 4 of 6 step 1 / "register" output
```
        : L             DW 1
        : L             KF 1
        : ><F
        : SPB           =M001
        : L             DW 2           - output "register"
        : T             MB 201
        : L             KT 0010.0
        : SE            =TD
        : UN            =TD            - if timer expires
        : SPB           =M001          then further testing
        : R             M 212.7        - reset to start parity bit
        : L             MB 200         and input data
        : T             MW 214         temporarily take over
        : S             M 214.5        set flag bit
M003    : UN            M 215.0
        : SPB           =M002
        : UN            M 212.7        - toggle parity depending on the data bit
        : =             M 212.7
M002    : L             MW 214
        : SRW           1
        : T             MW 214
        : UN            M 214.0        - if not done then loop
```

```
           : SPB          =M003
           : UN           M 212.7        - check whether parity o.k.
           : SPB          =M004          if no then end
           : L            DW 2           - load vector register
           : T            MW 214
           : U            M 215.0        - save bit
           : =            M 212.7
           : SRW          1              divide by 2
           : I            9              increase by 9
           : T            MW 214
           : U            M 212.7        - which tetrad?
           : SPB          =M005
           : B            MW 214         - low tetrad
           : L            DR 0           enter
           : L            KH 00F0
           : UW
           : L            MB 200
           : SLW          12
           : SRW          12
           : OW
           : B            MW 214
           : T            DR 0
           : SPA          =M006
M005 : B                  MW 214         - high tetrad
           : L            DR 0           enter
           : L            KH 000F
           : UW
           : L            MB 200
           : SLW          12
           : SRW          8
           : OW
           : B            MW 214
           : T            DR 0
M006 : L                  DW 2           - next register
           : I            1
           : T            DW 2
M004 : L                  KF 0           - error handling
           : T            DW 1           return jump
M001 : ***
network 5 of 6 register limit
           : L            KF 14          *** last register (14) ***
           : L            DW 2
           : >=F
           : U(
           : L            KF 0           01 *** first register +1 (1) ***
           : >F                          01
           : )                           01
```

```
        : SPB          =M001
        : L            KF 1
        : T            DW 2
M001 : ***
network 6 of 6
        : BE
```

# 7 Technical data

| | |
|---|---|
| **Supply voltage:** | 24V DC +/- 20% |
| **Power consumption:** | 3 watt |
| **Display:** | 4 status-LEDs |
| **Handling/Configuration:** | DIP-Switch |
| **Interfaces:** | **to the PLC:**<br>5 x screw type terminal for E/A-inputs<br>5 x screw type terminal for E/A-outputs<br>**others:**<br>2 x screw type terminal for 24V/DC power supply<br>15pol female for DCF77-antenna connection |
| **Operating temperature:** | 0 - 55°C |
| **Case:** | powder coated metal case with mounting flange |
| **Dimensions:** | 97 x 149 x 36 mm |
| **Scope of delivery:** | |
| | SPS-CLOCK |

## 7.1 Pin 15pin. antenna connection

| pin number | short form | description | direction |
|---|---|---|---|
| 1 | GNDA | screen | |
| 4 | +5V | +5V power supply | exit |
| 5 | GND | mass | exit |
| 8 | GNDA | screen | |
| 10 | DCF-IN | DCF signal receiving line | input |